3)

a)

Address	Problem 1		Problem 2	
	tag (24 bits)	block index (3 bits)	tag (25 bits)	set index (3 bits)
0x0	0x0	0x0	0x0	0x0
0x4	0x0	0x0	0x0	0x0
0x100	0x1	0x0	0x2	0x0
0x120	0x1	0x1	0x2	0x2
0x420	0x4	0x1	0x8	0x2
0x430	0x4	0x1	0x8	0x3

b)

Problem 1:

0x0	tag=0, block=0	cold miss
0x4	tag=0, block=0	hit
0x100	tag=1, block=0	conflict miss
0x120	tag=1, block=1	cold miss
0x420	tag=4, block=1	conflict miss
0x430	tag=4, block=1	hit

$$miss\ rate = \frac{misses}{memory\ accesses} = \frac{4}{6} = 66.\dot{6}\%$$

Problem 2:

0x0	tag=0, set=0	cold miss (way #0)
0x4	tag=0, set=0	hit
0x100	tag=2, set=0	cold miss (way #1)
0x120	tag=2, set=2	cold miss (way #0)
0x420	tag=8, set=2	cold miss (way #1)
0x430	tag=8, set=3	cold miss (way #0)

$$miss\ rate\ (MR) = \frac{misses}{memory\ accesses} = \frac{5}{6} = 83.\dot{3}\%$$

c)

Compute the AMAT of trace T on the two cache architectures if tCache = 1 cycle and tMMEM = 300 cycles.

Problem 1:

$$AMAT = t_{Cache} + MR \cdot t_{MMEM} = 1 + \frac{4}{6} \cdot 300 = 201$$

Problem 2:

$$AMAT = t_{Cache} + MR \cdot t_{MMEM} = 1 + \frac{5}{6} \cdot 300 = 251$$

d)

Compute the AMAT of trace T on the two cache architectures if tCache = 1 cycle, tMMEM = 300 cycles, and we include an L2 cache with a miss rate of 5% of the L1 misses and tL2 = 10 cycles.

Problem 1:

$$AMAT = t_{Cache} + MR_{L1} \cdot (t_{L2} + MR_{L2} \cdot t_{MMEM}) = 1 + \frac{4}{6} \cdot (10 + 5\% \cdot 300) = 17.\dot{6}$$

Problem 2:

$$AMAT = t_{Cache} + MR_{L1} \cdot (t_{L2} + MR_{L2} \cdot t_{MMEM}) = 1 + \frac{5}{6} \cdot (10 + 5\% \cdot 300) = 21.8\dot{3}$$